CLAIMS

What is claimed is:

1. A method of performing model to hardware correlation, comprising:

simulating models based upon design criteria;

manufacturing devices based upon said design criteria;

evaluating features of said devices during said manufacturing to produce in-line test parametric data;

comparing said models to said in-line test parametric data to obtain correlation data; and

modifying said simulating according to said correlation data.

2. The method in claim 1, wherein said simulating produces geometric, DC, AC, and delay stage simulated parameters, and

wherein said in-line test parametric data includes geometric, DC, AC, and delay stage test parameters.

3. The method in claim 1, wherein said modifying produces a modified simulation and said method further comprises identifying, in a characterization map, ones of said devices that match models produced by said modified simulation.

4. The method in claim 1, wherein:

said devices comprise semiconductor devices;

said models include modeled threshold voltage values;

said in-line test parametric data includes test threshold voltage values;

said comparing compares said modeled threshold voltage values and said test threshold voltage values to produce a threshold voltage adder; and

said modifying includes adding said threshold voltage adder to said modeled threshold voltage values.

5. The method in claim 1, wherein:

said devices comprise semiconductor devices;

said models include modeled saturated current values;

said in-line test parametric data includes test saturated current values;

said comparing compares said modeled saturated current values and said test saturation saturated current values to produce a saturated current error value.

6. The method in claim 1, wherein:

said devices comprise semiconductor devices;

said models include modeled delay per stage values;

said in-line test parametric data includes test delay per stage values;

said comparing compares said modeled delay per stage values and said test saturation delay per stage values to produce a delay per stage error value.

7. The method in claim 1, further comprising culling said in-line test parametric data to retain selected geometric, D.C., A.C. and delay test parameters.

8. The method in claim 1, further comprising identifying defective devices and removing said defective devices from said in-line test parametric data.

9. A method of correcting a hardware modeling process, said method comprising:

manufacturing devices based on design criteria;

measuring features of said devices to produce measured features;

isolating a portion of said modeling process;

supplying at least one of said measured features to said portion of said modeling process, wherein said portion of said modeling process outputs a simulated result;

comparing said simulated result to a corresponding measured feature of said measured features; and

calculating a correction to said portion of said modeling process based on said comparing.

10. The method in claim 9, wherein said simulated result and said corresponding measured feature comprise one of a voltage, current, and physical dimension.

11. The method in claim 9, wherein said portion of said modeling process simulates an integrated circuit design to model one of saturation threshold voltage, saturated source/drain current, and delay per stage.

12. The method in claim 9, further comprising repeating said method for second portions of said modeling process to produce second corrections.

13. The method in claim 12, further comprising modifying said modeling process based on said correction and said second corrections, such that said modeling process automatically makes said corrections after performing a simulation.

14. The method in claim 9, wherein said measuring comprises measuring physical dimensions and performance operations of said devices at different points of said manufacturing of said devices.

15. The method in claim 9, further comprising performing a statistical analysis based on results of said comparing process.

16. A method of performing model to hardware correlation for semiconductor chips, comprising:

obtaining fabrication in-line parametric data;

extracting first parameters from said parametric data to make a first set of go-data;

calculating a first simulated threshold voltage saturation and first simulated saturated source/drain current based on said first set of go-data using a modeling program;

performing a first comparing of said first simulated threshold voltage saturation to an in-line parametric threshold voltage saturation from said parametric data and a first comparing of said first simulated saturated source/drain current to an in-line parametric saturated source/drain current from said parametric data;

calculating a threshold voltage adder from said first comparing; and

correcting said modeling program using said threshold voltage adder.

17. The method in claim 16, further comprising

adding said threshold voltage adder to said first set of go-data to make a second set of go-data;

calculating a second simulated threshold voltage saturation and second simulated saturated source/drain current based on said second set of go-data using said modeling program;

performing a second comparing of said second simulated threshold voltage saturation to said in-line parametric threshold voltage saturation and a second comparing of said second simulated saturated source/drain current to said in-line parametric saturated source/drain current; and

verifying that said threshold voltage adder corrected said second simulated threshold voltage saturation and said second simulated saturated source/drain current.

18. The method in claim 17, further comprising calculating a percentage error based on said second comparing process and adding said percentage error to said second set of go-data to make a third set of go-data.

19. The method in claim 18, further comprising:

calculating a simulated delay-per-stage based on said third set of go-data using said modeling program;

performing a third comparing of said simulated delay-per-stage to an in-line parametric delay-per-stage from said parametric data; and

calculating a delay-per-stage error based on said third comparing process.

20. The method in claim 19, further comprising:

adding said delay-per-stage error to said third set of go-data to make a final set of go-data; and

outputting statistics based on said threshold voltage adder, said percentage error and said delay-per-stage error.

21. The method in claim 18, further comprising:

performing a fourth comparing of parametric yield data from said final set of go-data to functional yield data from wafer final test servers;

selecting acceptable chips which have good parametric yield data and good functional yield data from said fourth comparing process; and

creating a model to hardware wafer map showing locations of said acceptable chips.

22. The method in claim 21, further comprising performing a model to hardware comparison using said model to hardware wafer map.

23. The method in claim 16, further comprising, after said extracting, removing defective chips from said first parameters to make said first set of go-data.

24. A method of performing model to hardware correlation for semiconductor chips, comprising:

obtaining fabrication in-line parametric data;

extracting first parameters from said parametric data to make a first set of go-data;

calculating a first simulated threshold voltage saturation and first simulated saturated source/drain current based on said first set of go-data using a modeling program;

performing a first comparing of said first simulated threshold voltage saturation to an in-line parametric threshold voltage saturation from said parametric data and a first comparing of said first simulated saturated source/drain current to an in-line parametric saturated source/drain current from said parametric data;

calculating a threshold voltage adder from said first comparing;

adding said threshold voltage adder to said first set of go-data to make a second set of go-data;

calculating a second simulated threshold voltage saturation and second simulated saturated source/drain current based on said second set of go-data using said modeling program;

performing a second comparing of said second simulated threshold voltage saturation to said in-line parametric threshold voltage saturation and a second comparing of said second simulated saturated source/drain current to said in-line parametric saturated source/drain current;

calculating a percentage error based on said second comparing process and adding said percentage error to said second set of go-data to make a third set of go-data;

calculating a simulated delay-per-stage based on said third set of go-data using said modeling program;

performing a third comparing of said simulated delay-per-stage to an in-line parametric delay-per-stage from said parametric data;

calculating a delay-per-stage error based on said third comparing process;

adding said delay-per-stage error to said third set of go-data to make a final set of go-data; and

correcting said modeling program using said final set of go-data.

25. The method in claim 24, further comprising, after said extracting, removing defective chips from said first parameters to make said first set of go-data.

26. The method in claim 24, further comprising, after said second comparing, verifying that said threshold voltage adder corrected said second simulated threshold voltage saturation and said second simulated saturated source/drain current.

27. The method in claim 24, further comprising outputting statistics based on said threshold voltage adder, said percentage error and said delay-per-stage error.

28. The method in claim 24, further comprising:

performing a fourth comparing of parametric yield data from said final set of go-data to functional yield data from wafer final test servers;

selecting acceptable chips which have good parametric yield data and good functional yield data from said fourth comparing process;

creating a model to hardware wafer map showing locations of said acceptable chips; and

performing a model to hardware comparison using said model to hardware wafer map.

29. A method of performing model to hardware correlation for semiconductor chips, comprising:

obtaining fabrication line parametric data;

extracting first parameters from said parametric data;

removing defective chips from said first parameters to make a first set of go-data;

calculating a first simulated threshold voltage saturation and first simulated saturated source/drain current based on said first set of go-data using a modeling program;

performing a first comparing of said first simulated threshold voltage saturation to an in-line parametric threshold voltage saturation from said parametric data and a first comparing of said first simulated saturated source/drain current to an in-line parametric saturated source/drain current from said parametric data;

calculating a threshold voltage adder from said first comparing;

adding said threshold voltage adder to said first set of go-data to make a second set of go-data;

calculating a second simulated threshold voltage saturation and second simulated saturated source/drain current based on said second set of go-data using said modeling program;

performing a second comparing of said second simulated threshold voltage saturation to said in-line parametric threshold voltage saturation and a second comparing of said second simulated saturated source/drain current to said in-line parametric saturated source/drain current;

verifying that said threshold voltage adder corrected said second simulated threshold voltage saturation and said second simulated saturated source/drain current;

calculating a percentage error based on said second comparing process and adding said percentage error to said second set of go-data to make a third set of go-data;

calculating a simulated delay-per-stage based on said third set of go-data using said modeling program;

performing a third comparing of said simulated delay-per-stage to an in-line parametric delay-per-stage from said parametric data;

calculating a delay-per-stage error based on said third comparing process;

adding said delay-per-stage error to said third set of go-data to make a final set of go-data;

outputting statistics based on said threshold voltage adder, said percentage error and said delay-per-stage error;

performing a fourth comparing of parametric yield data from said final set of go-data to functional yield data from wafer final test servers;

selecting acceptable chips which have good parametric yield data and good functional yield data from said fourth comparing process;

creating a model to hardware wafer map showing locations of said acceptable chips; and

performing a model to hardware comparison using said model to hardware wafer map.

30. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for performing model to hardware correlation, comprising:

simulating models based upon design criteria;

manufacturing devices based upon said design criteria;

evaluating features of said devices during said manufacturing to produce in-line test parametric data;

comparing said models to said in-line test parametric data to obtain correlation data; and

modifying said simulating according to said correlation data.

31. The program storage device as claimed in claim 30, wherein said simulating produces geometric, DC, AC, and delay stage simulated parameters, and

wherein said in-line test parametric data includes geometric, DC, AC, and delay stage test parameters.

32. The program storage device as claimed in claim 30, wherein said modifying produces a modified simulation and said method further comprises identifying, in a characterization map, ones of said devices that match models produced by said modified simulation.

33. The program storage device as claimed method in claim 30, wherein:

said devices comprise semiconductor devices;

said models include modeled threshold voltage values;

said in-line test parametric data includes test threshold voltage values;

said comparing compares said modeled threshold voltage values and said test threshold voltage values to produce a threshold voltage adder; and

said modifying includes adding said threshold voltage adder to said modeled threshold voltage values.

34. The program storage device as claimed method in claim 30, wherein:

said devices comprise semiconductor devices;

said models include modeled saturated current values;

said in-line test parametric data includes test saturated current values;

said comparing compares said modeled saturated current values and said test saturation saturated current values to produce a saturated current error value.

35. The program storage device as claimed method in claim 30, wherein:

said devices comprise semiconductor devices;

said models include modeled delay per stage values;

said in-line test parametric data includes test delay per stage values;

said comparing compares said modeled delay per stage values and said test saturation delay per stage values to produce a delay per stage error value.

36. The program storage device as claimed method in claim 30, further comprising culling said in-line test parametric data to retain selected geometric, D.C., A.C. and delay test parameters.